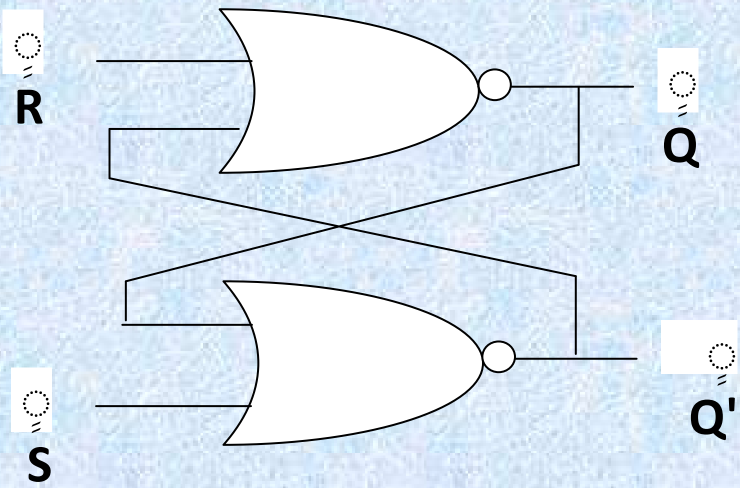
Chapter 2

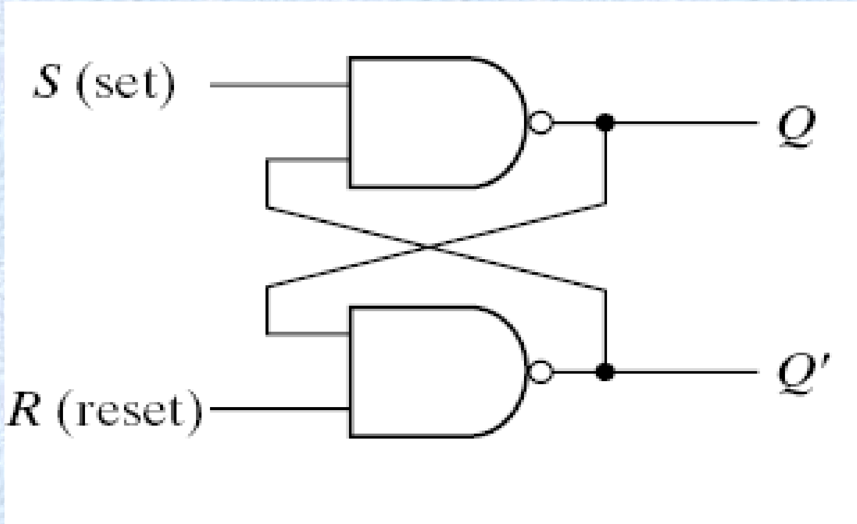
Sequential Circuits and Flip-flops

The R-S flip-flop



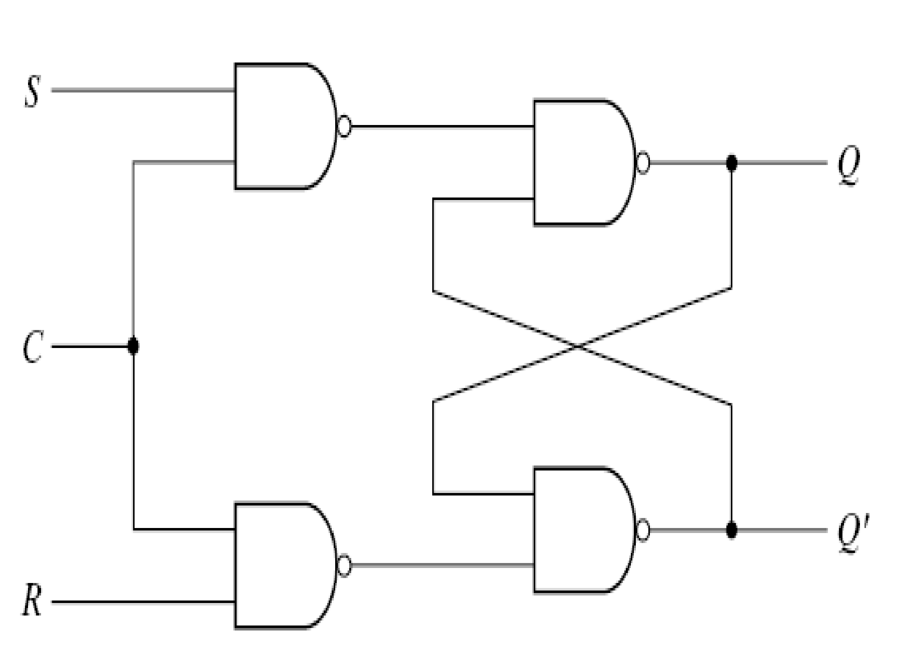
S	R	Q	Q'
1	0	1	0
0	0	1	0 (after SR= 10)
0	1	0	1
0	0	0	1(after SR=01)
1	1	0	0 (Disallowed)

The R-S flip-flop



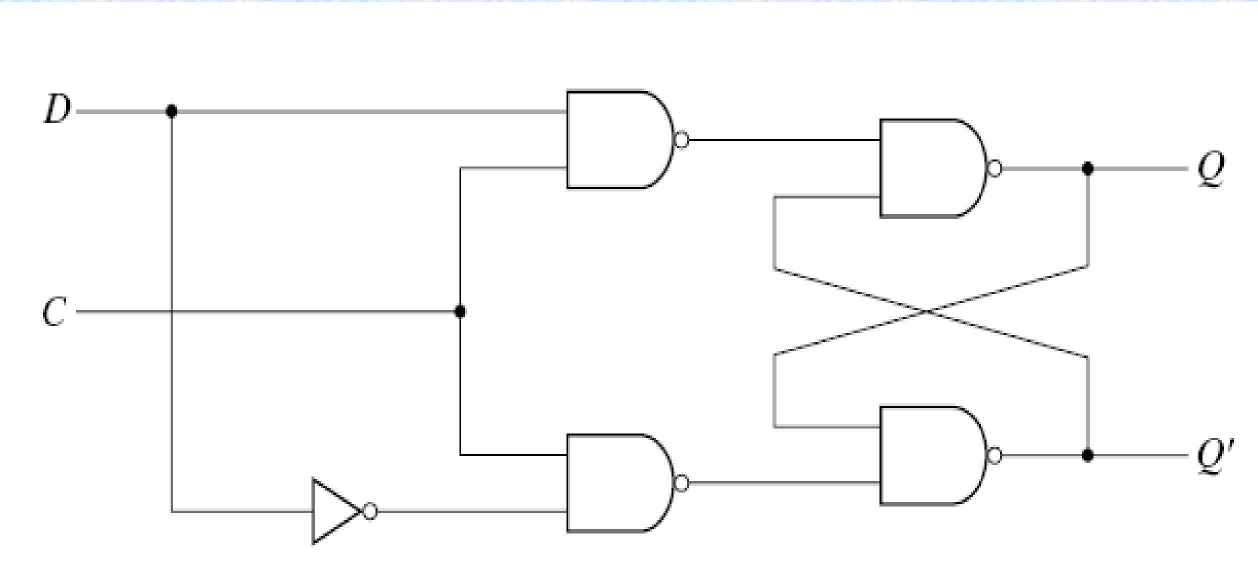
S	R	Q	Q'
1	0	0	1
1	1	0	1 (after SR= 10)
0	1	1	0
1	1	1	0(after SR=01)
0	0	1	1 (Disallowed)

The clocked R-S flip-flop

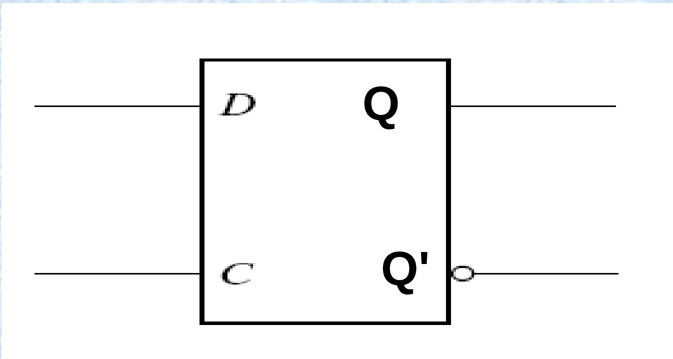


C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; set state
1	1	1	Indeterminate

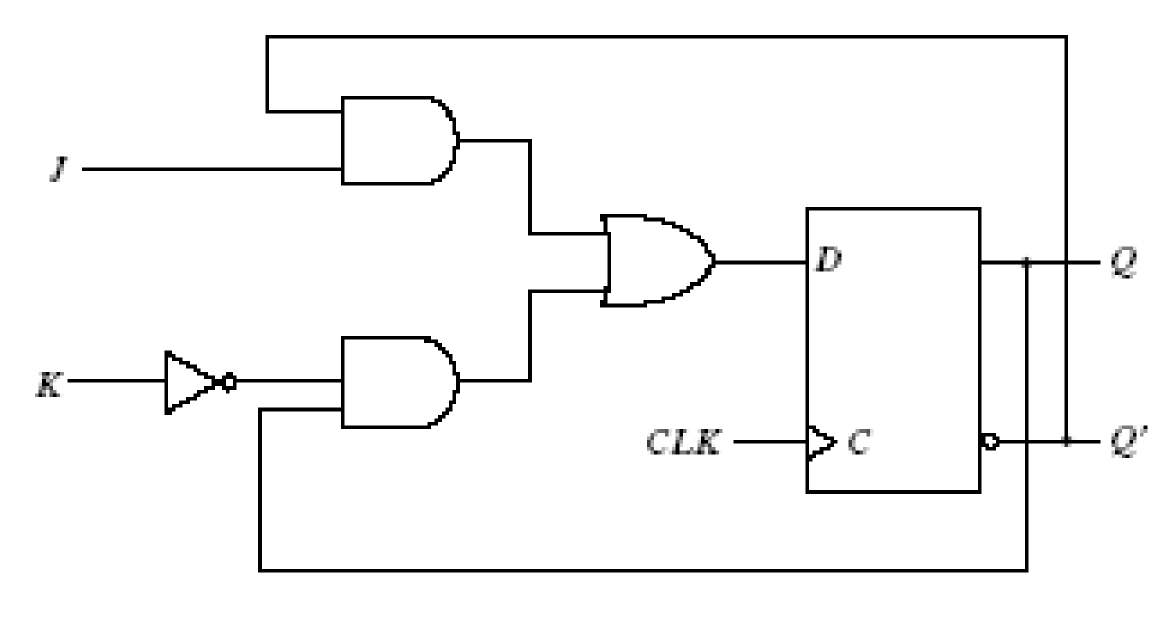
D flip-flop

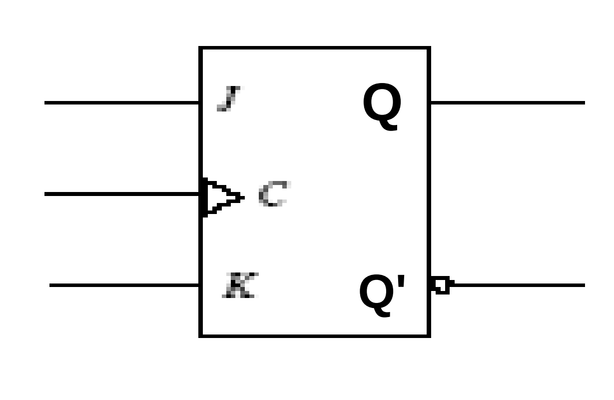


D	Q(t+1)
0	0
1	1



JK flip-flop

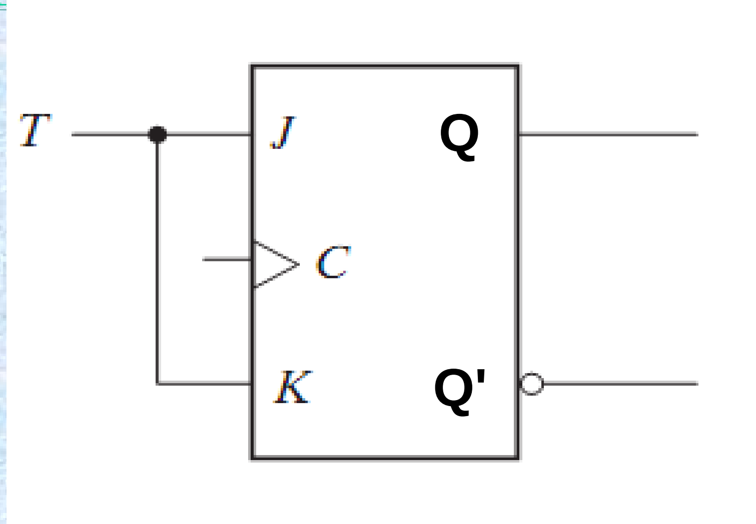


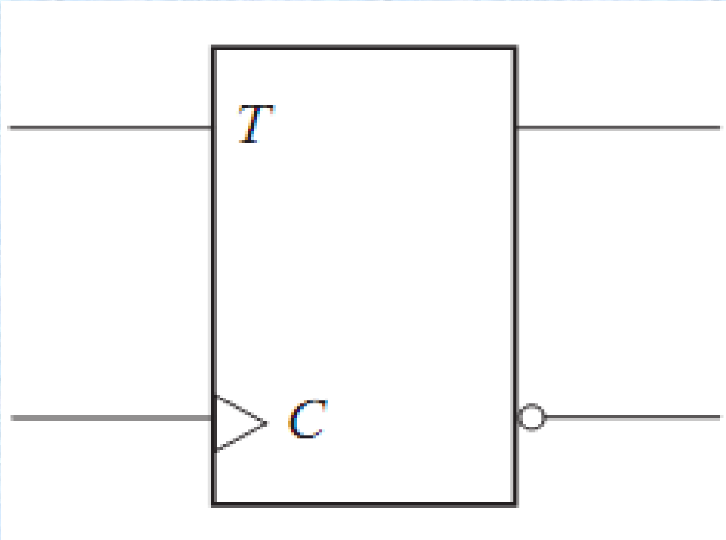


J	K	Q(t+1)
0	0	No change in state
0	1	0
1	0	1
1	1	Complement state

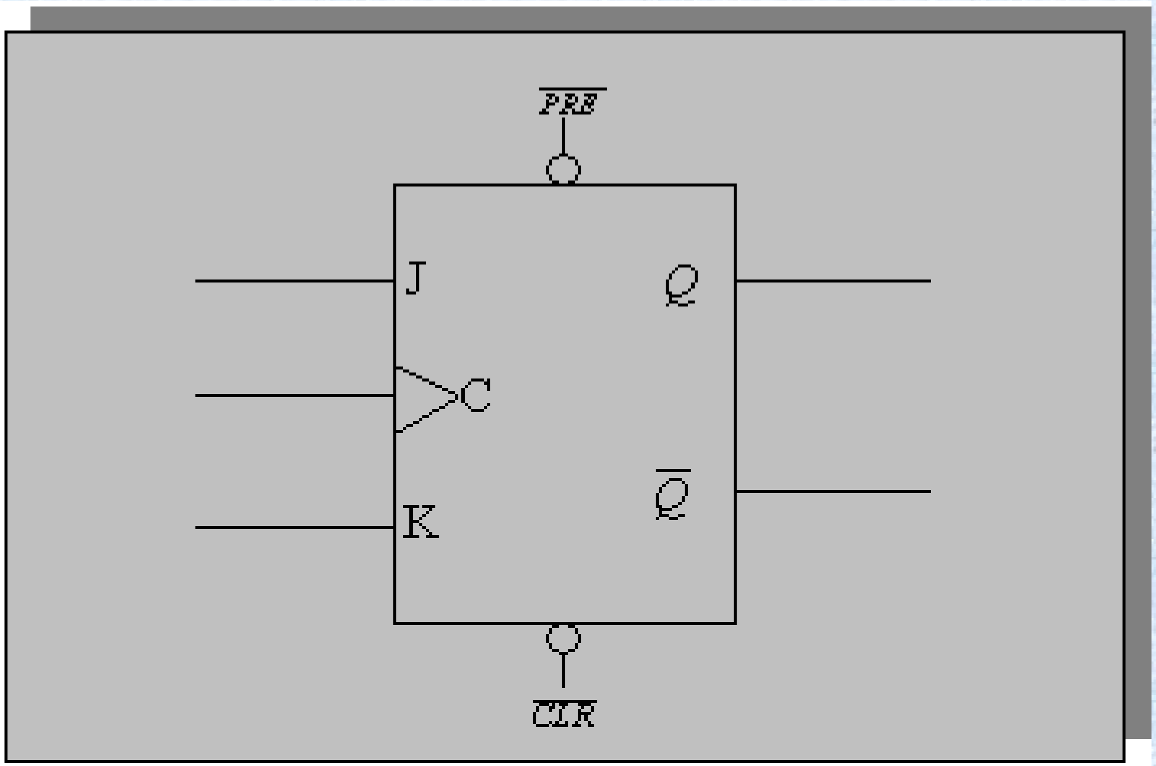
T flip-flop

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

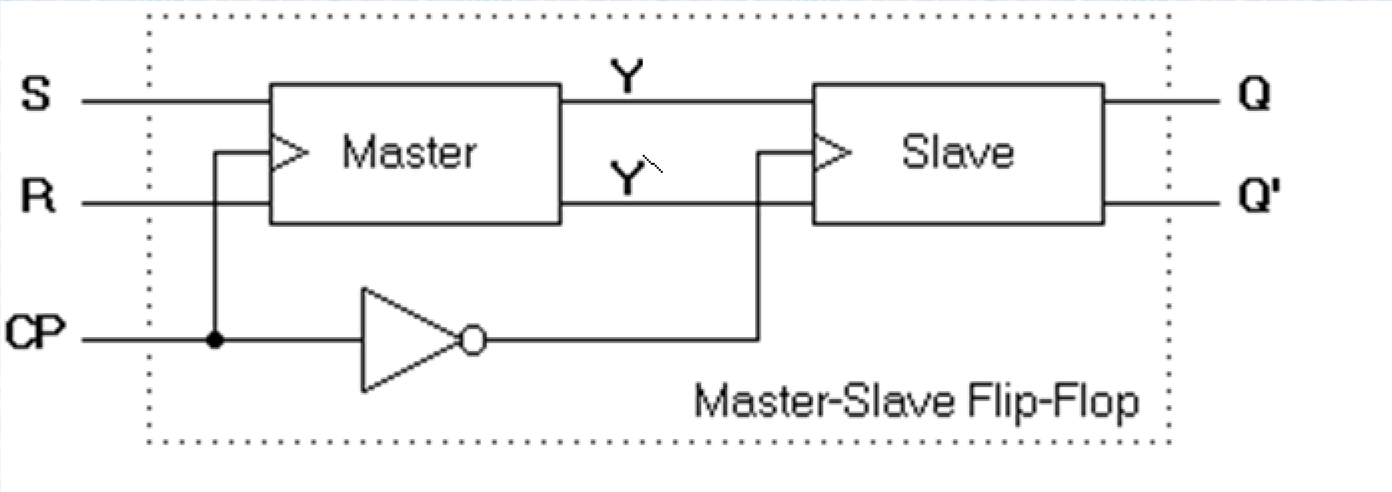


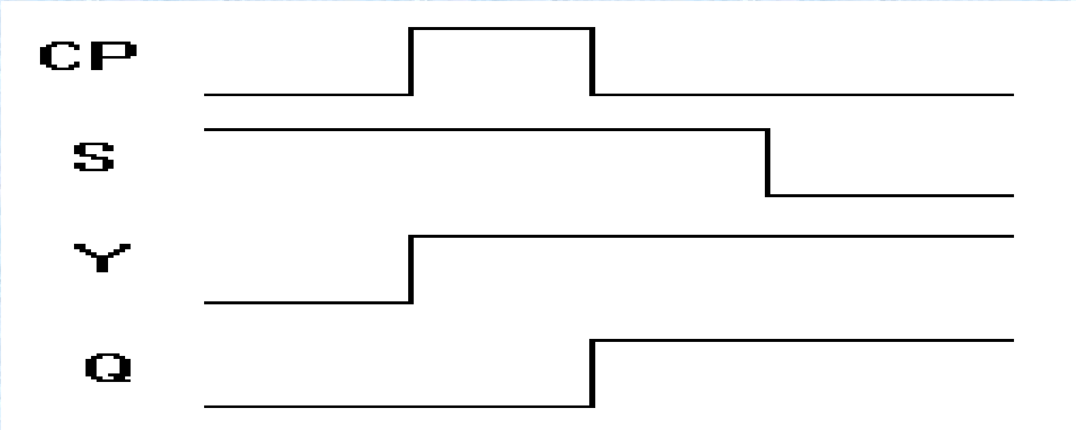


Flip Flops - with asynchronous inputs



Master-Slave Flip-Flop





Sequential circuit analysis

- State table
- State diagram
- Timing diagram

What is a "state"?

- **The value of the outputs of the flip-flops simultaneously at a given period of time (usually measured after the CP edge arrival).**

- **Thus if we have two flip-flops, there output will be expressed in two bits (00, 01, 10 and 11)**

What is present state and next state?

- **<u>Present state</u> is the value of flip-flop output before the arrival of the CP edge.**

- **<u>Next state</u> is the value of flip-flop output after the arrival of the CP edge.**

-

State table

Present State		Next State		Output
Q1(t)	Q2(t)	Q1(t+1)	Q2(t+1)	Y
0	0	0	1	1
0	1	1	0	1
1	0	1	1	0
1	1	0	0	1

Read this state table

Quiz (oral)

Present State		Next State		Output
Q1(t)	Q2(t)	Q1(t+1)	Q2(t+1)	Y(t)
0	0	0	1	1
0	1	1	1	0
1	0	0	0	1
1	1	1	0	0

Read this state table

Present State		Input	Next State		Output
Q1(t)	Q2(t)	X	Q1(t+1)	Q2(t+1)	Y
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	1
1	1	0	1	0	0
1	1	1	0	0	1

1- Assume we begin at state Q1=0 and Q2=0.
2- X=0, the next state (Q1=0 and Q2=0) producing Y=1.
3- X=1, the next state (Q1=0 and Q2=1) producing Y=1.

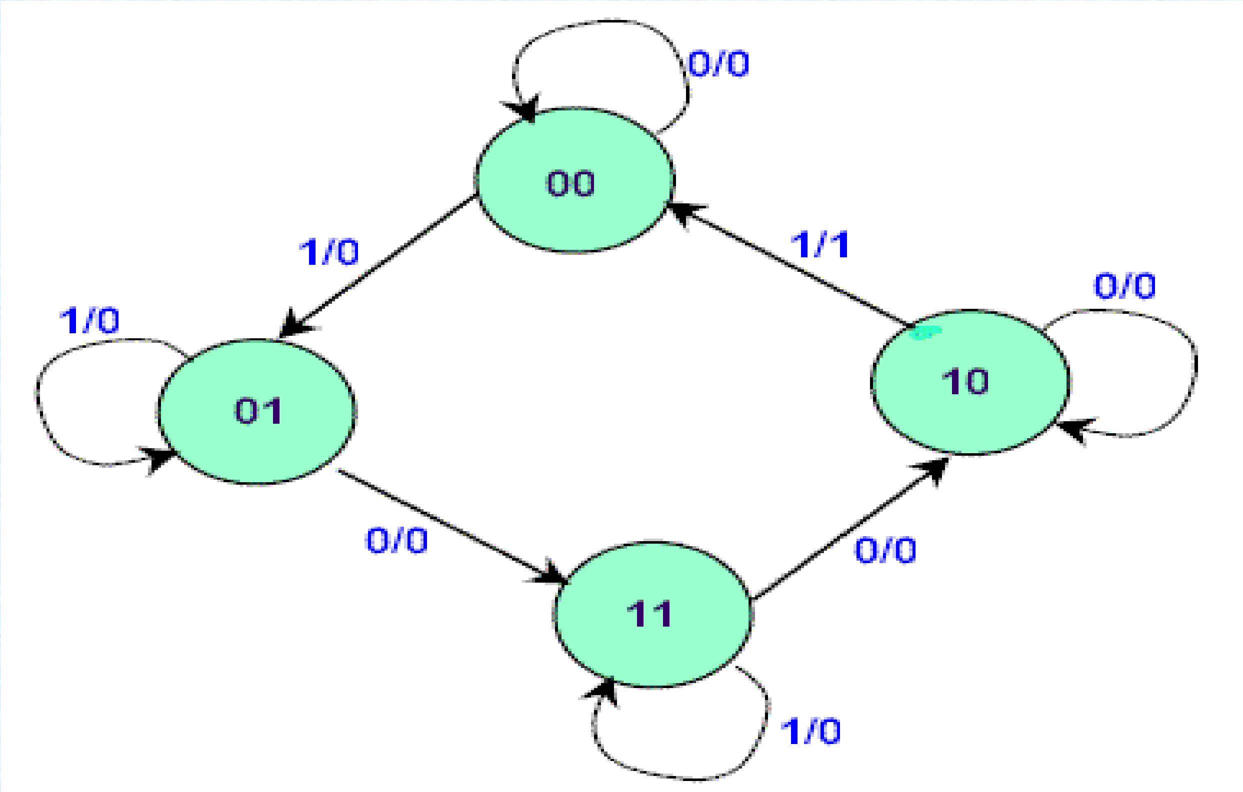
Now, can you deduce the next state of the following cases:

- **(Q1=1 and Q2=0) and the input X=0**
- **(Q1=1 and Q2=0) and the input X=1**
- **(Q1=1 and Q2=1) and the input X=0**

Another version of the state table

Present State		Next State X=0		Next State X=1		Output Y(t)	
Q1(t)	Q2(t)	Q1(t+1)	Q2(t+1)	Q1(t+1)	Q2(t+1)	X=0	X=1
0	0	0	0	0	1	1	1
0	1	1	0	0	0	0	1
1	0	1	1	0	1	0	1
1	1	1	0	0	0	0	1

State Diagram



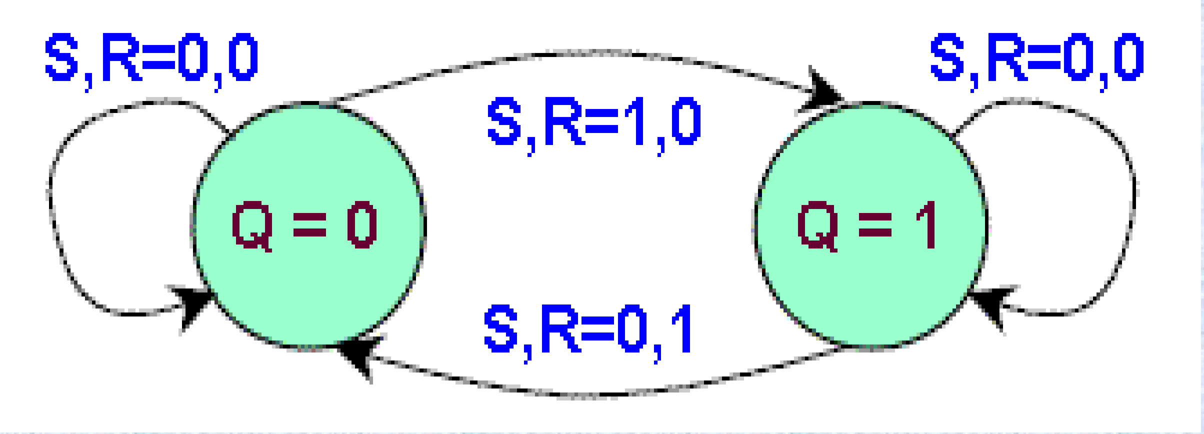
Now, can you deduce the next state of the following cases:

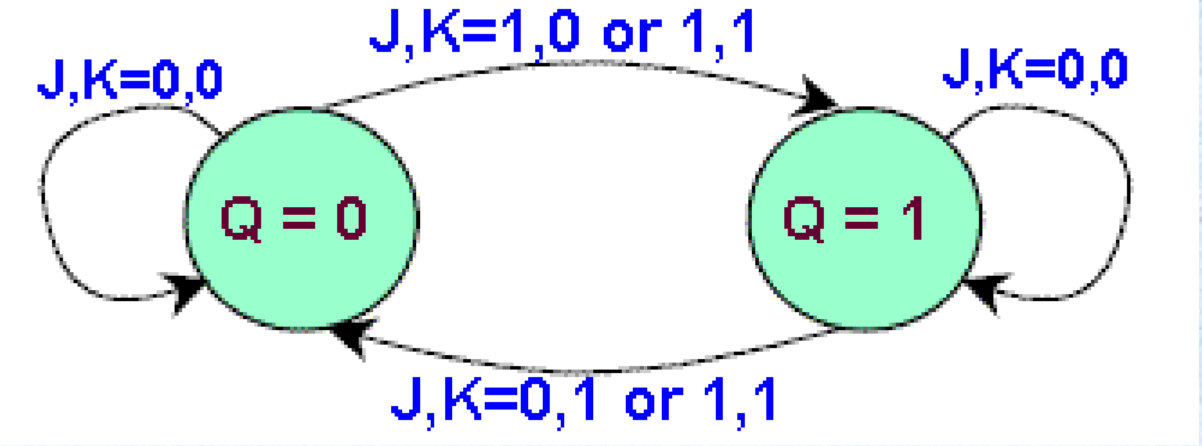
- **Present state 11 and the input =0**

- **Present state 11 and the input =1**

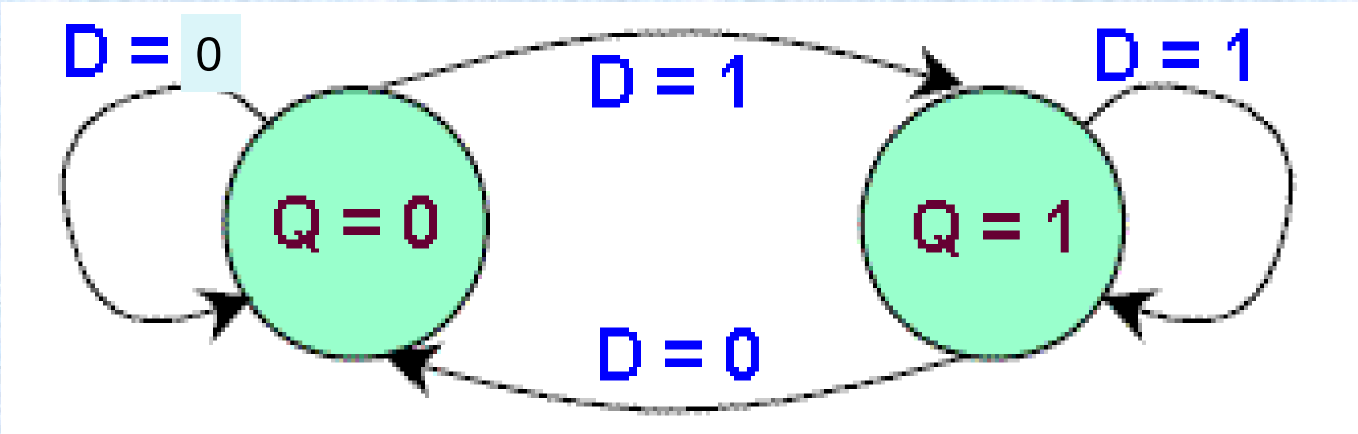
- **Present state 10 and the input =0**

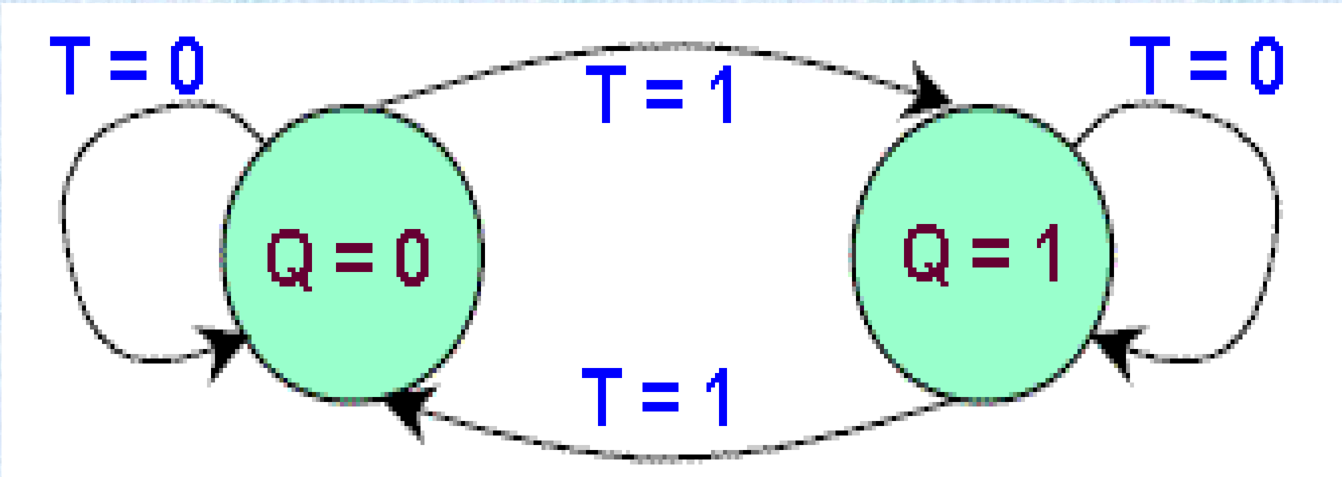
State Diagrams of Various Flip-flops





State Diagrams of Various Flip-flops

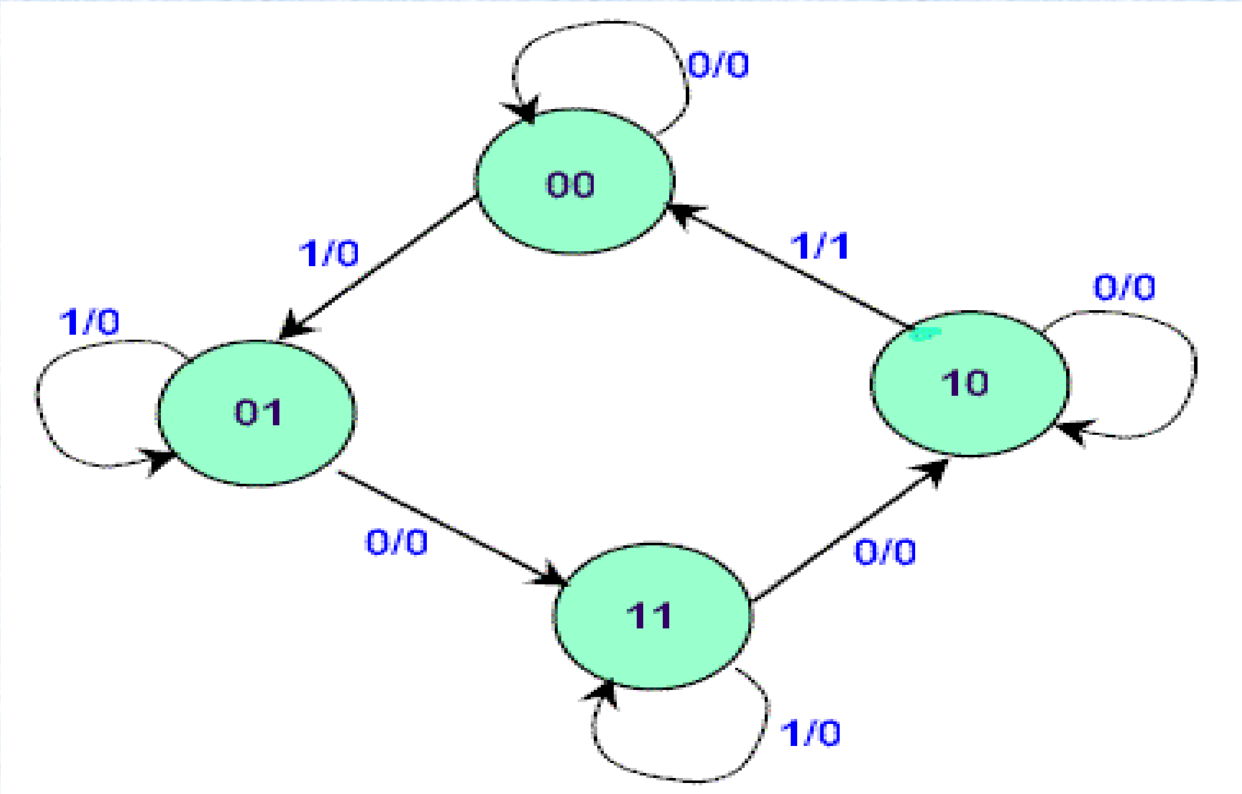




Converting from state diagram into state table

Present State Q1(t)	Q2(t)	Next State X=0 Q1(t+1)	Q2(t+1)	Next State X=1 Q1(t+1)	Q2(t+1)	Output Y(t) X=0	X=1
0	0	0	0	0	1	1	1
0	1	1	0	0	0	0	1
1	0	1	1	0	1	0	1
1	1	1	0	0	0	0	1

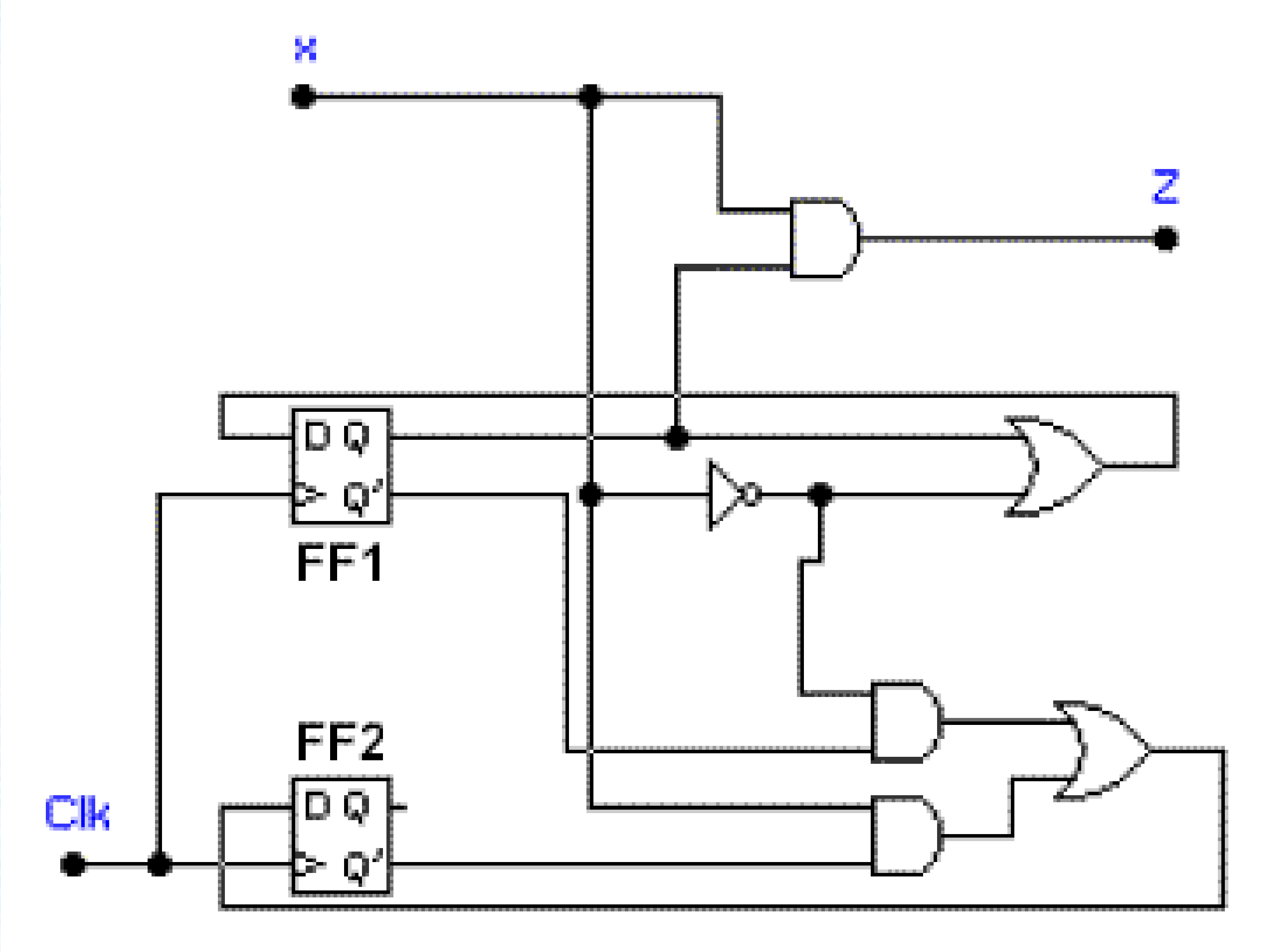
Converting from state diagram into state table



Sequential Circuit Analysis

- We start with the logic diagram of the circuit which we can derive the input equations for each flip-flop.
- Then, to obtain next-state equations according to the input equations and the type of flip-flop.
- The output variable(s) equations can also be derived from the schematic, and once we have our output and next-state equations, we can generate the next-state and output tables as well as state diagrams.

Example 1:

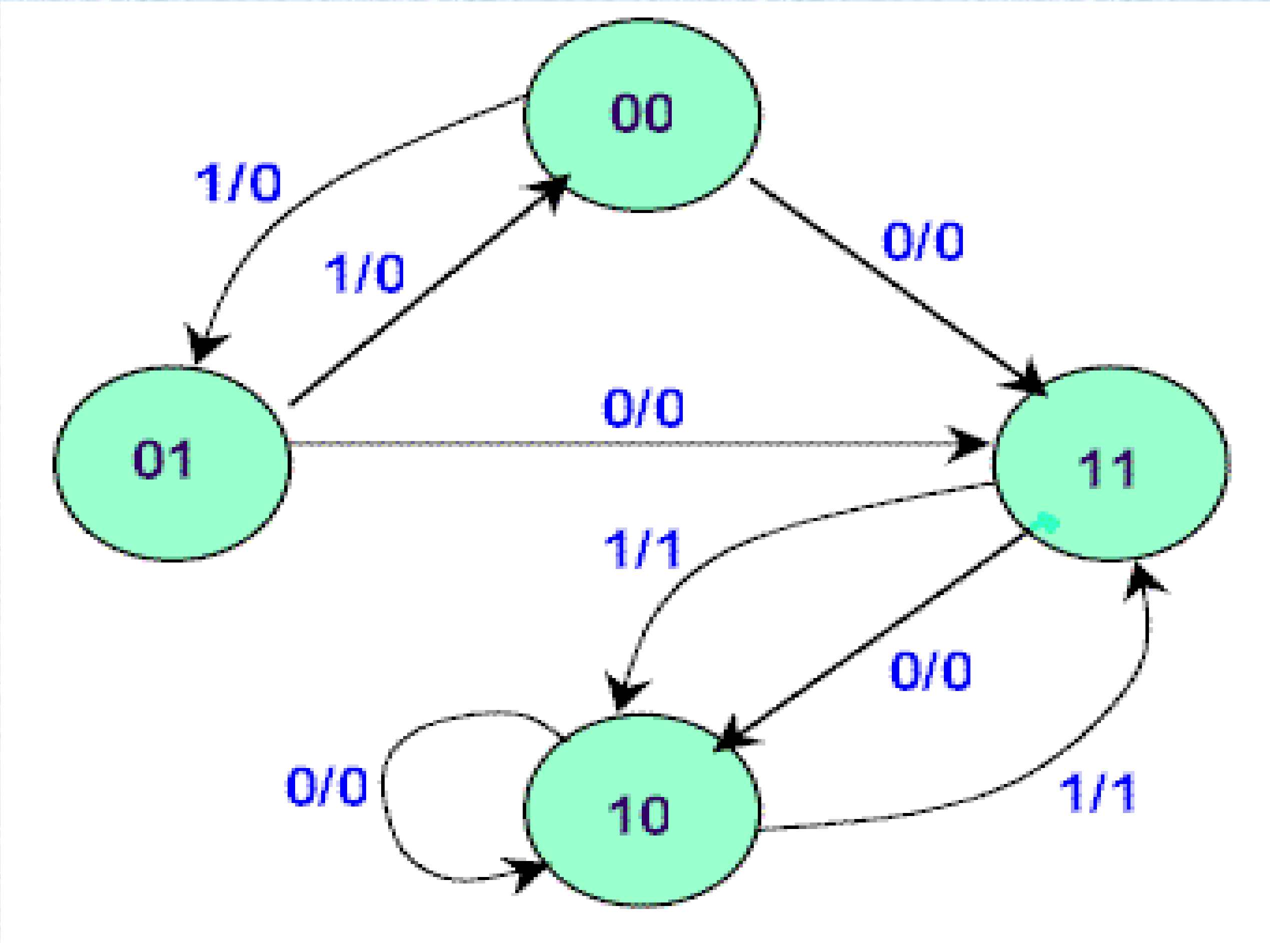


Example 1:

- From the figure, the inputs of the flip flops are:
- $D1 = X' + Q1$
- $D2 = X.Q2' + X'.Q1'$

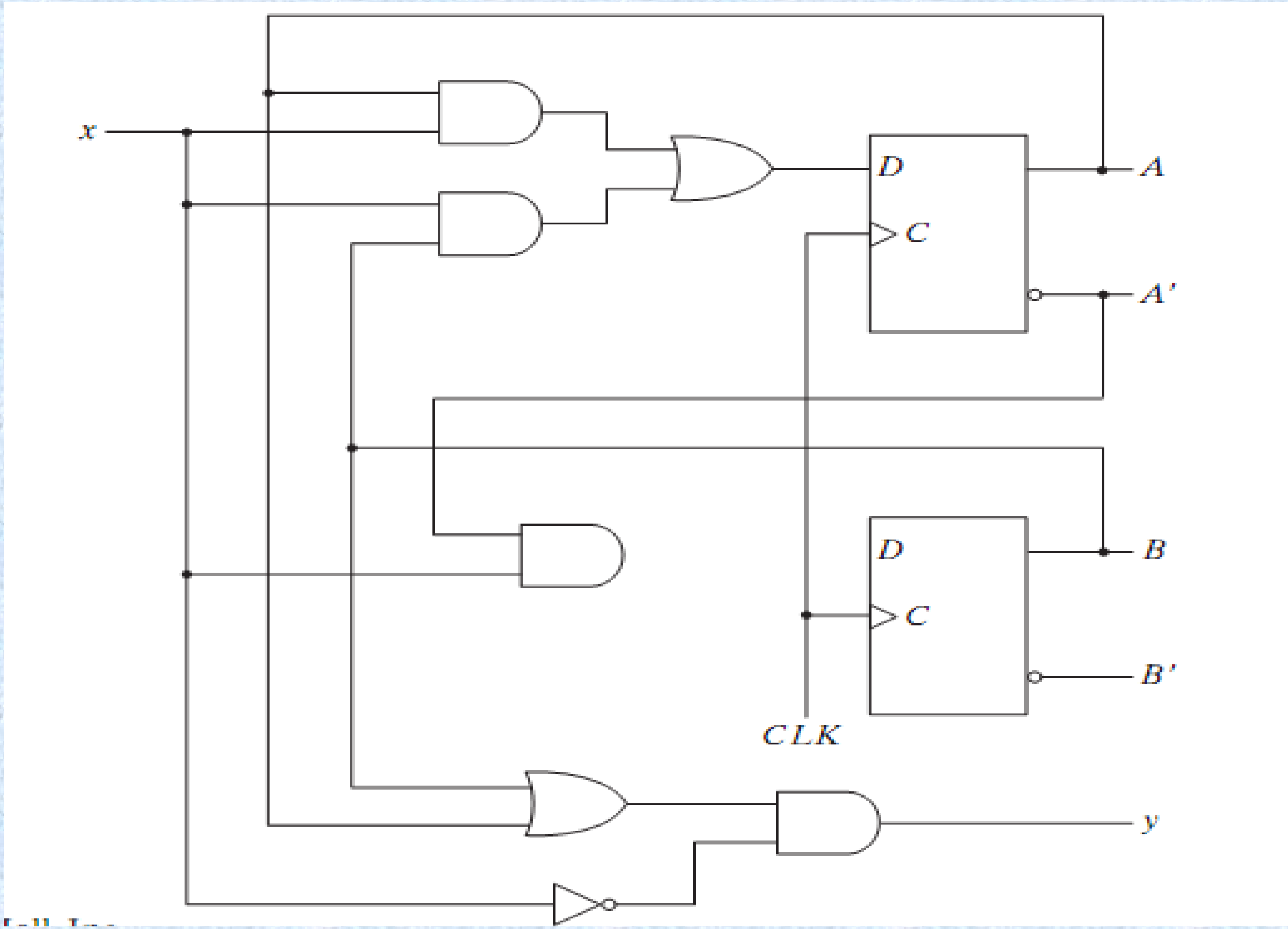
- The output Z equation is:
  - $Z = X*Q1$

Present State		Input	Next State		Output
Q1(t)	Q2(t)	X	Q1(t+1)	Q2(t+1)	Z
0	0	0	1	1	0
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			



00
1/0
1/0
0/0
01
0/0
11
1/1
0/0
0/0
10
1/1

Example 2:



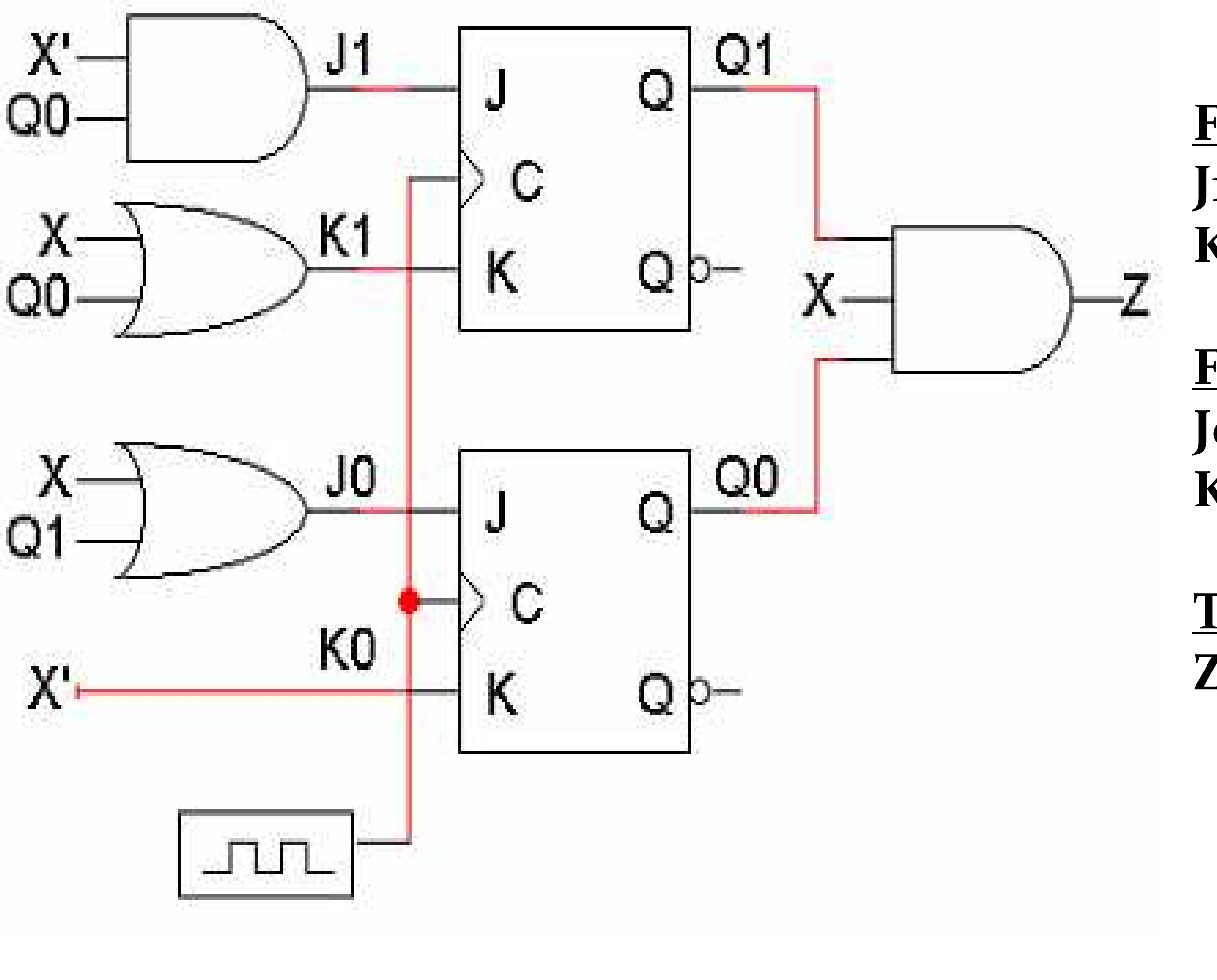
- **$A(t+1) = DA = A(t).X(t) + B(t).X(t)$**
- **$B(t+1) = DB = A'(t).X(t)$**
- The output Y equation is:

$Y(t) = X'(t).(B(t) + A(t))$

Present State		Input	Next State		Output
Q1(t)	Q2(t)	X	Q1(t+1)	Q2(t+1)	Z
0	0	0	0	0	0
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Present State	Next State		Output	
	x(t)=0	x(t)=1	x(t)=0	x(t)=1
A(t) B(t)	A(t+1)B(t+1)	A(t+1)B(t+1)	y(t)	y(t)
0 0	0 0	0 1	0	0
0 1	0 0	1 1	1	0
1 0	0 0	1 0	1	0
1 1	0 0	1 0	1	0

Example 3:



For the first flip flop:

J1 = X'(t). Qo(t)

K1 = X(t) + Qo(t)

For the second flip flop

Jo = X (t) + Q1(t)

Ko = X'(t)

The output

Z = Q1(t). X(t). Qo(t)

Present State		Inputs	Flip-flop Inputs			
Q_1	Q_0	X	J_1	K_1	J_0	K_0
0	0	0	0	0	0	1
0	0	1	0	1	1	0
0	1	0	1	1	0	1
0	1	1	0	1	1	0
1	0	0	0	0	1	1
1	0	1	0	1	1	0
1	1	0	1	1	1	1
1	1	1	0	1	1	0

Build the state table for PS, inputs and flip-flop inputs

Complete the state table for NS, using inputs and flip-flop inputs and excitation table

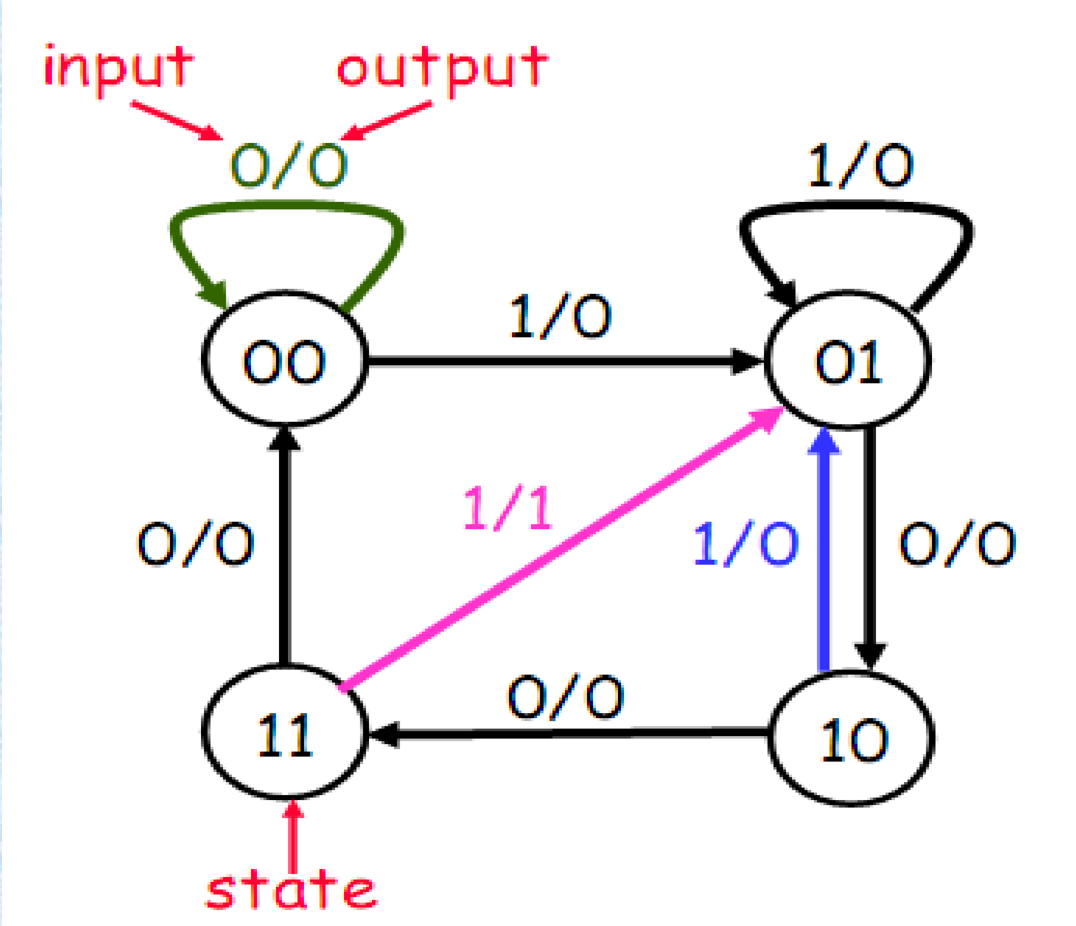
J	K	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

Present State		Inputs	FF Inputs				Next State	
Q_1	Q_0	X	J_1	K_1	J_0	K_0	Q_1	Q_0
0	0	0	0	0	0	1	0	0
0	0	1	0	1	1	0	0	1
0	1	0	1	1	0	1	1	0
0	1	1	0	1	1	0	0	1
1	0	0	0	0	1	1	1	1
1	0	1	0	1	1	0	0	1
1	1	0	1	1	1	1	0	0
1	1	1	0	1	1	0	0	1

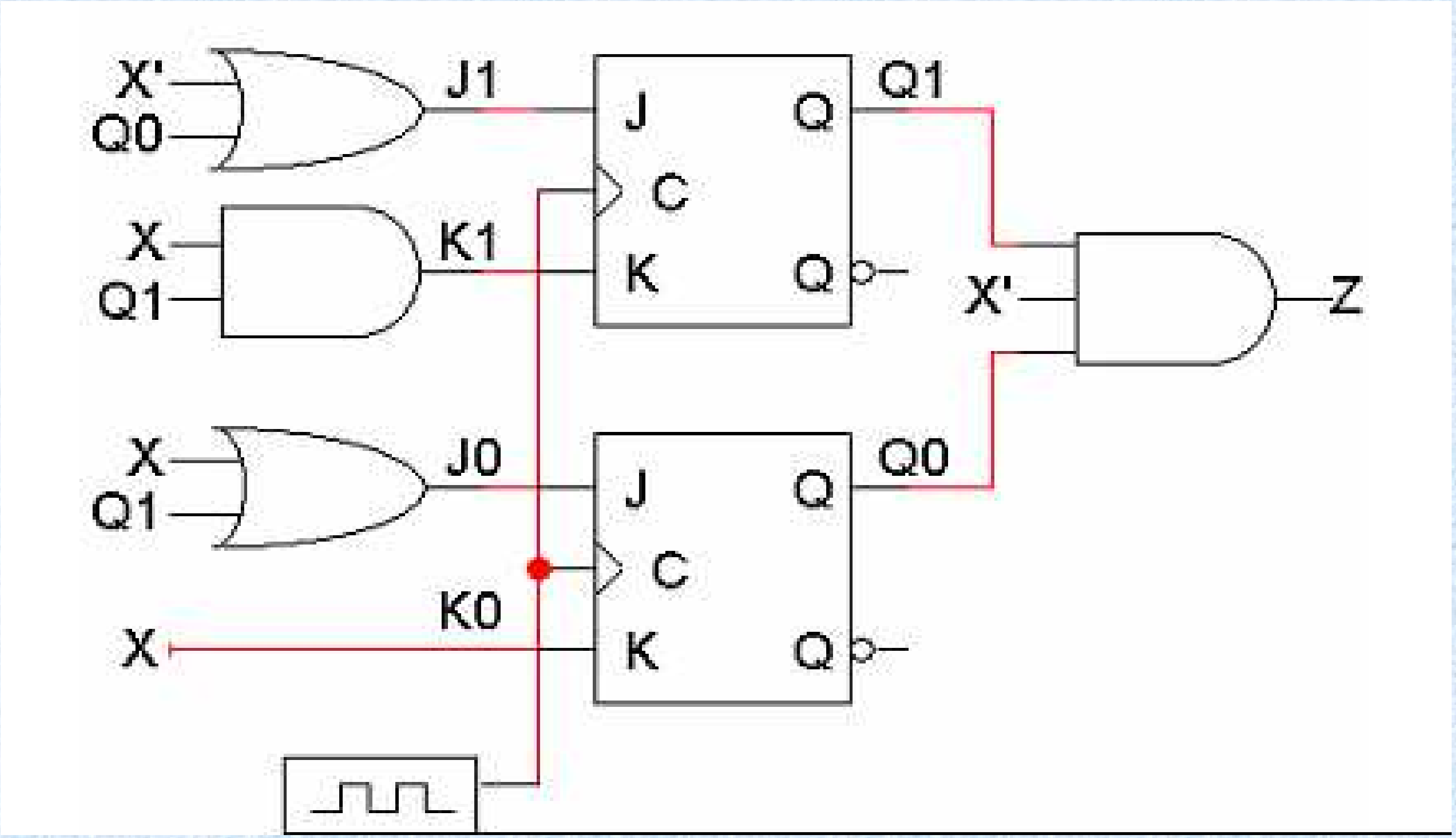
Complete the state table for output Z, using PS inputs and X input

Present State		Inputs	FF Inputs				Next State		Outputs
Q_1	Q_0	X	J_1	K_1	J_0	K_0	Q_1	Q_0	Z
0	0	0	0	0	0	1	0	0	0
0	0	1	0	1	1	0	0	1	0
0	1	0	1	1	0	1	1	0	0
0	1	1	0	1	1	0	0	1	0
1	0	0	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0	1	0
1	1	0	1	1	1	1	0	0	0
1	1	1	0	1	1	0	0	1	1

Draw the state diagram from state table

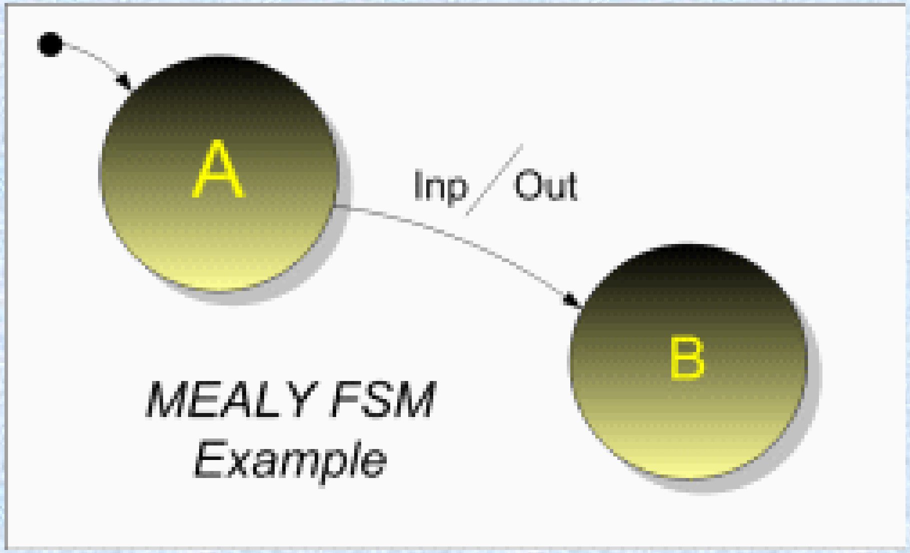


Report

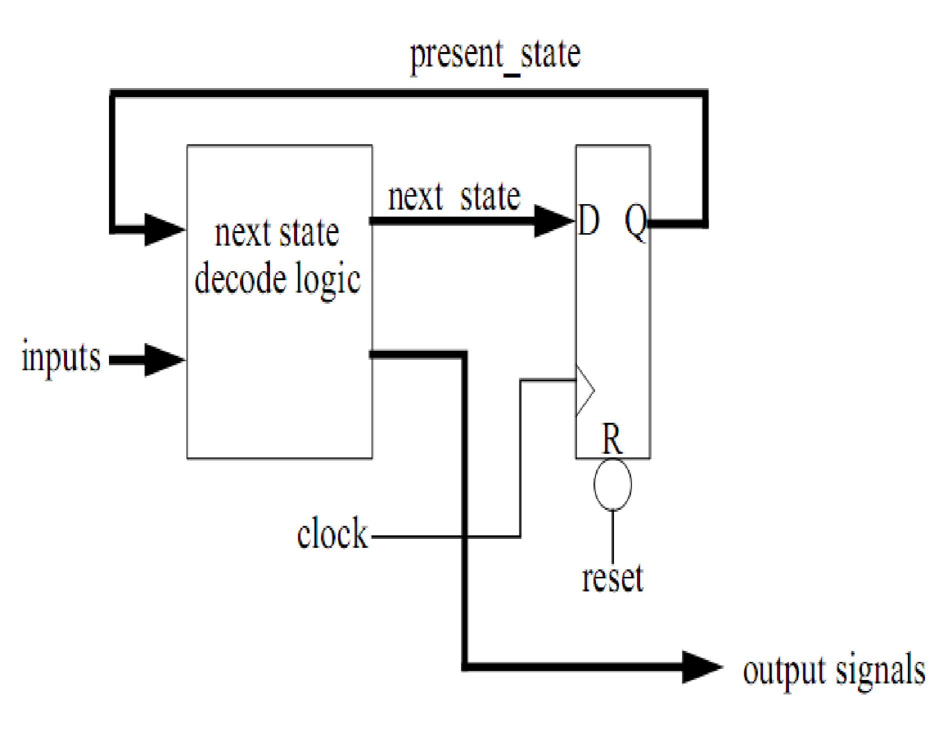


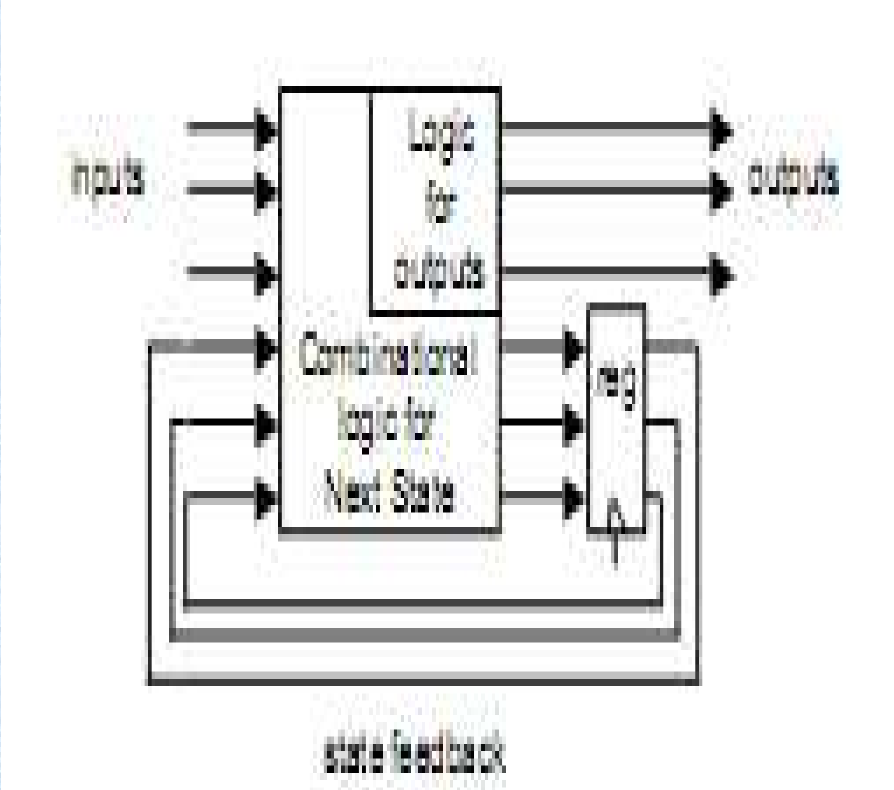
Mealy and Moore state diagrams

- A **Mealy circuit** (sometimes called **machine**) generates an output based on its current state *and* input. This means that the state diagram will include both input and output signals for each transition edge.

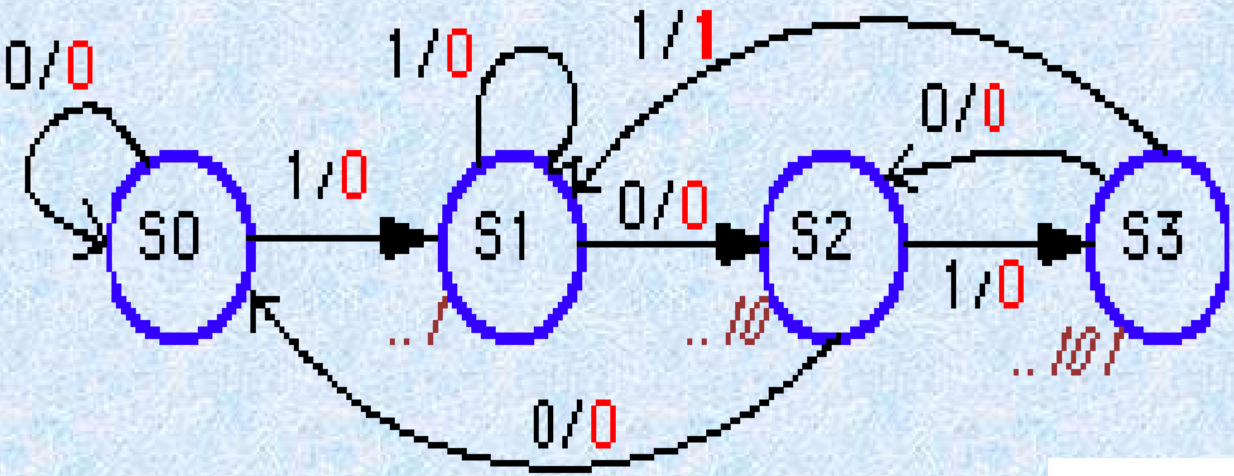


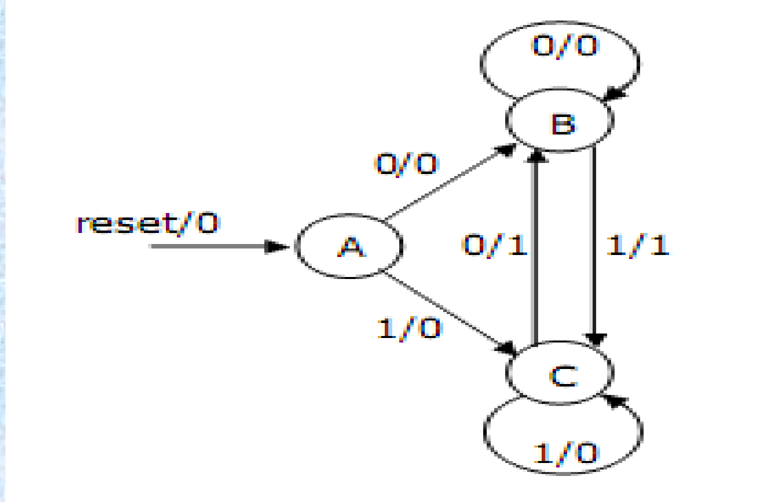
Mealy circuit

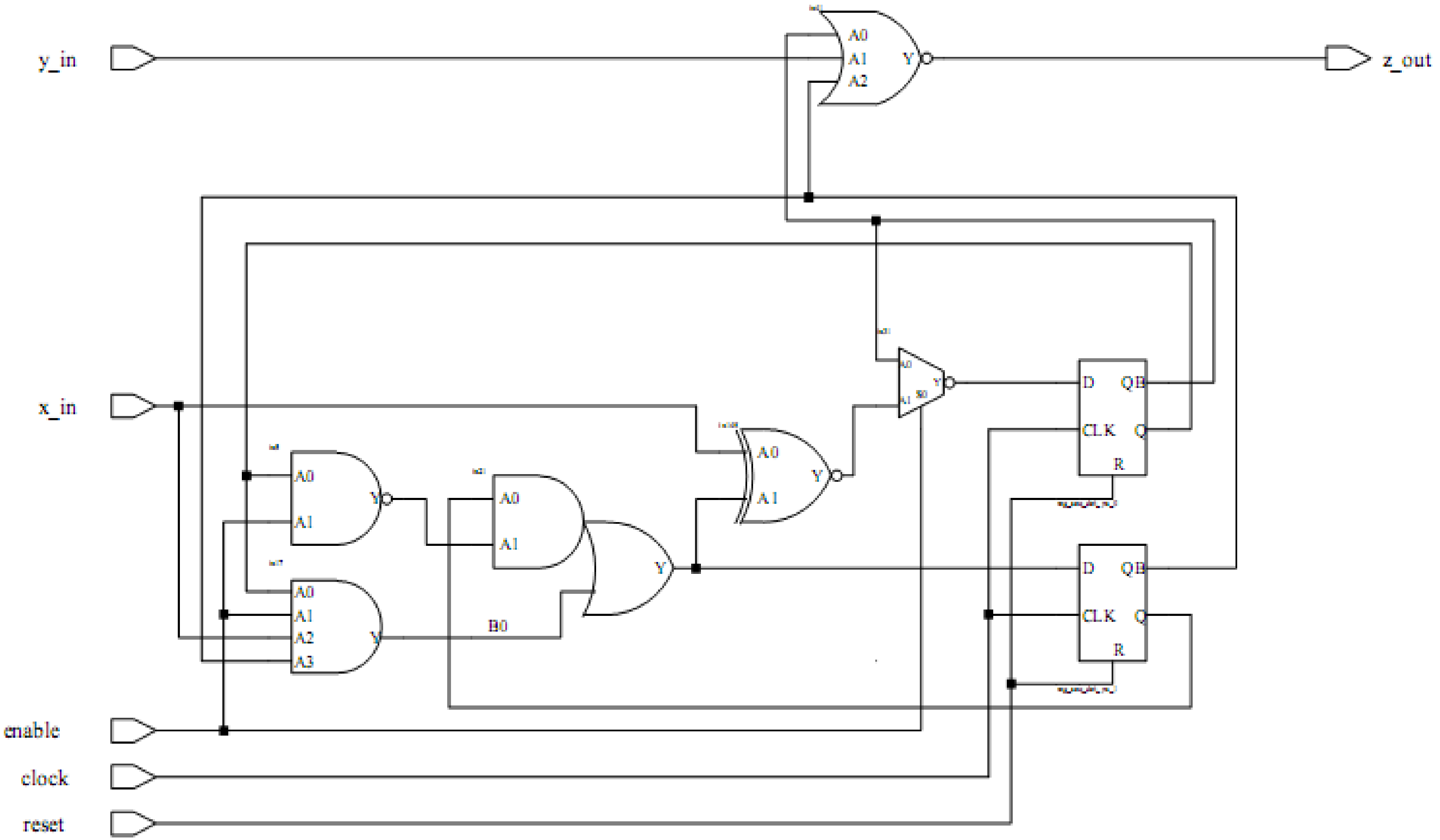




Mealy circuit

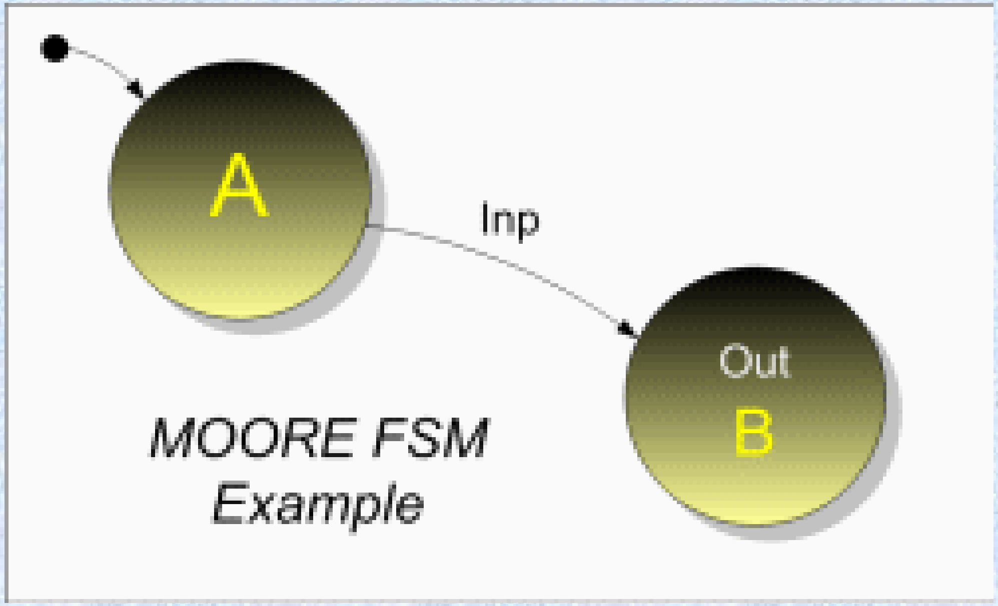




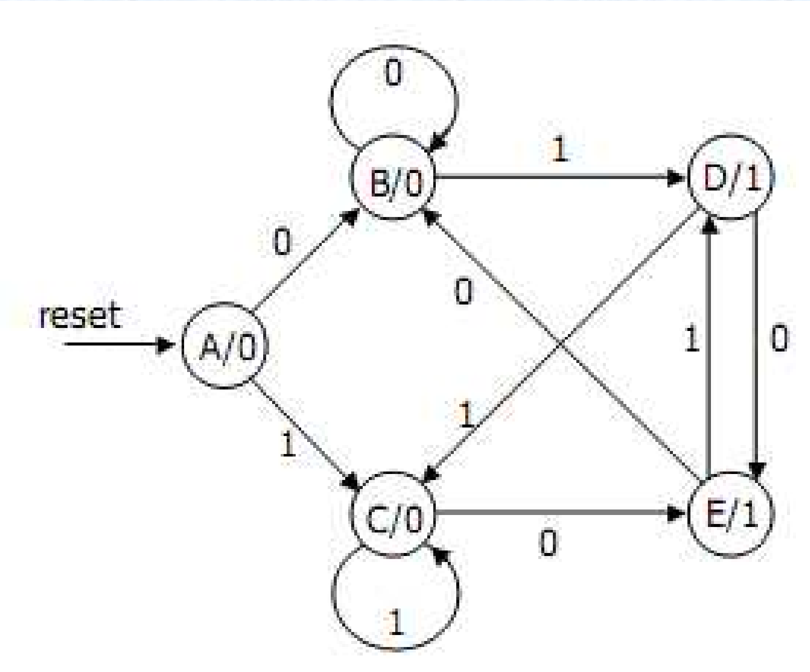

y_in
z_out
x_in
enable
clock
reset
A0
A1
A2
A3
Y
B0
D
QB
CLK
Q
R

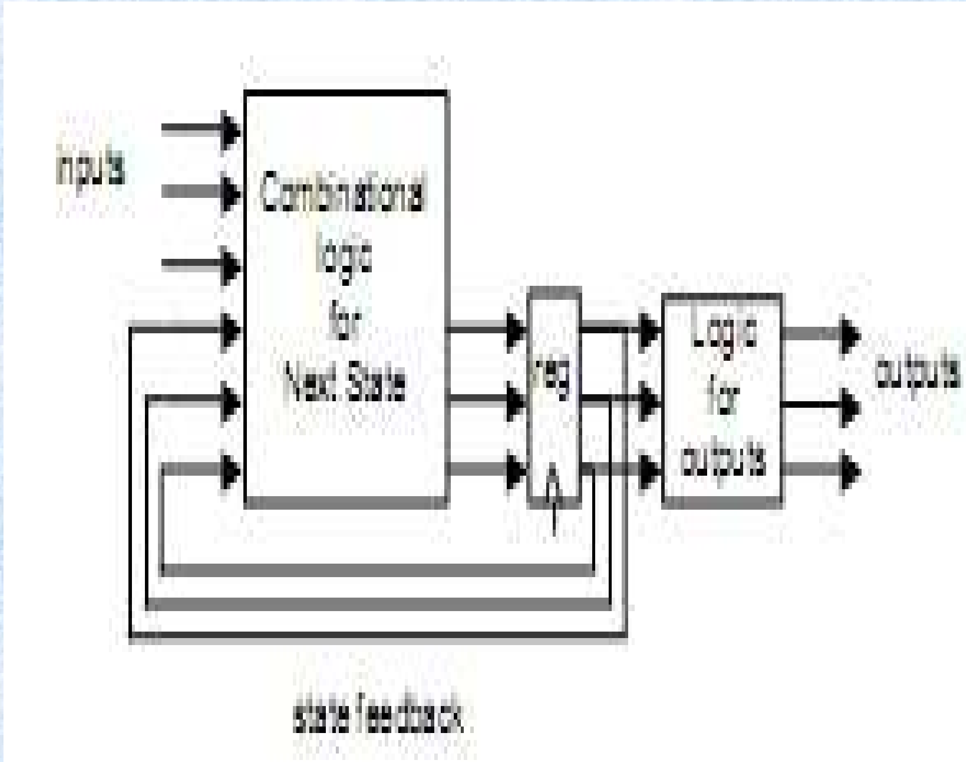
Moore circuit

- The output of a Moore finite state machine depends only on the machine's current state; transitions are not directly dependent upon input. The outputs react at the edges of clock pulse.

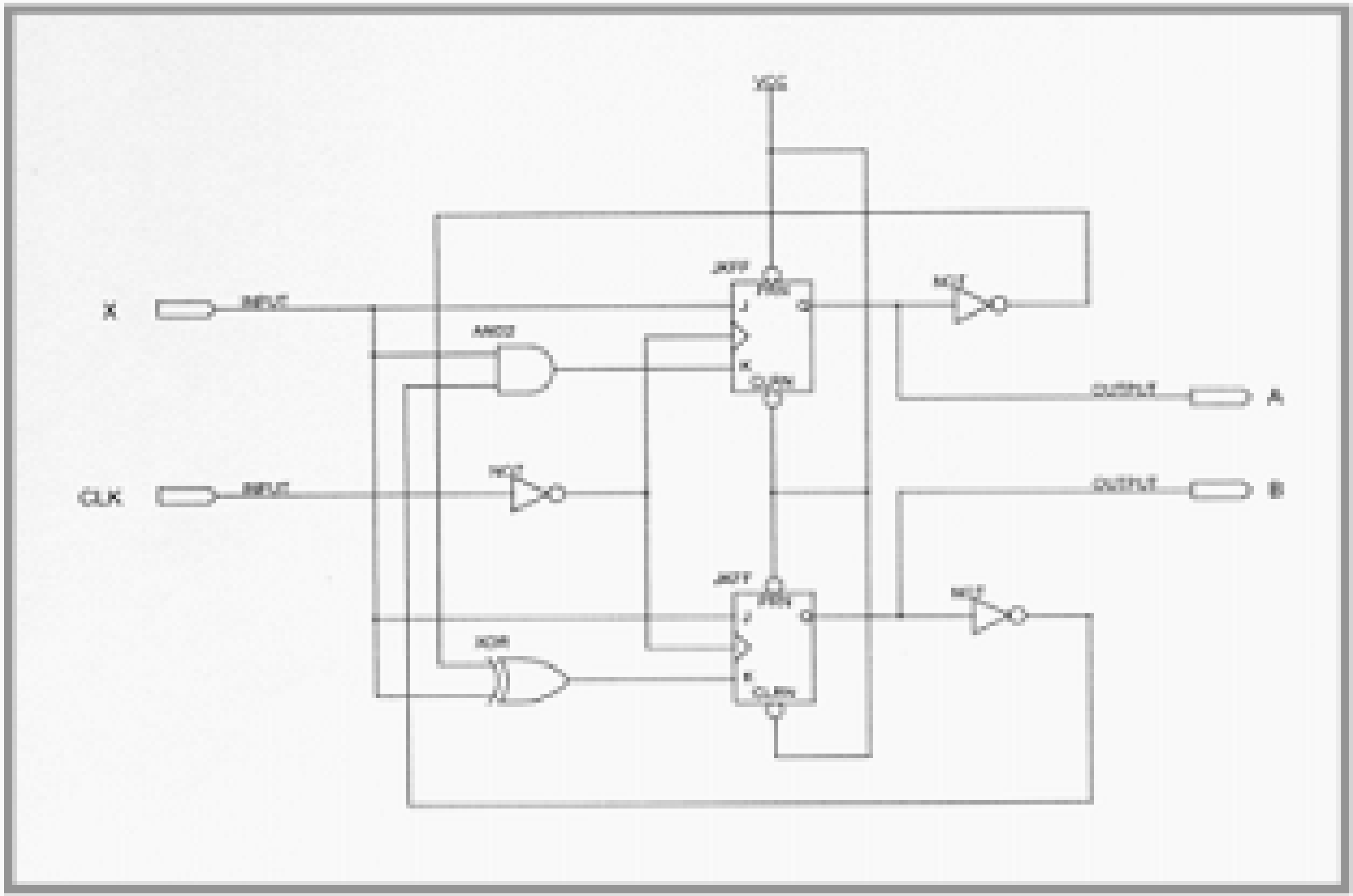


Moore circuit





Moore circuit



State diagram reduction and assignment

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
S0	S1	S2	0	0
S1	S3	S4	0	0
S2	S5	S6	0	0
S3	S7	S8	0	0
S4	S9	S10	0	0
S5	S11	S12	0	0
S6	S13	S14	0	0
S7	S0	S0	0	0
S8	S0	S0	0	0
S9	S0	S0	0	0
S10	S0	S0	1	0
S11	S0	S0	0	0
S12	S0	S0	1	0
S13	S0	S0	0	0
S14	S0	S0	0	0

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
S0	S1	S2	0	0
S1	S3	S4	0	0
S2	S5	S6	0	0
S3	S7	S8	0	0
S4	S9	SA	0	0
S5	S11	SA	0	0
S6	S13	S14	0	0
S7	S0	S0	0	0
S8	S0	S0	0	0
S9	S0	S0	0	0
S11	S0	S0	0	0
SA	S0	S0	1	0
S13	S0	S0	0	0
S14	S0	S0	0	0

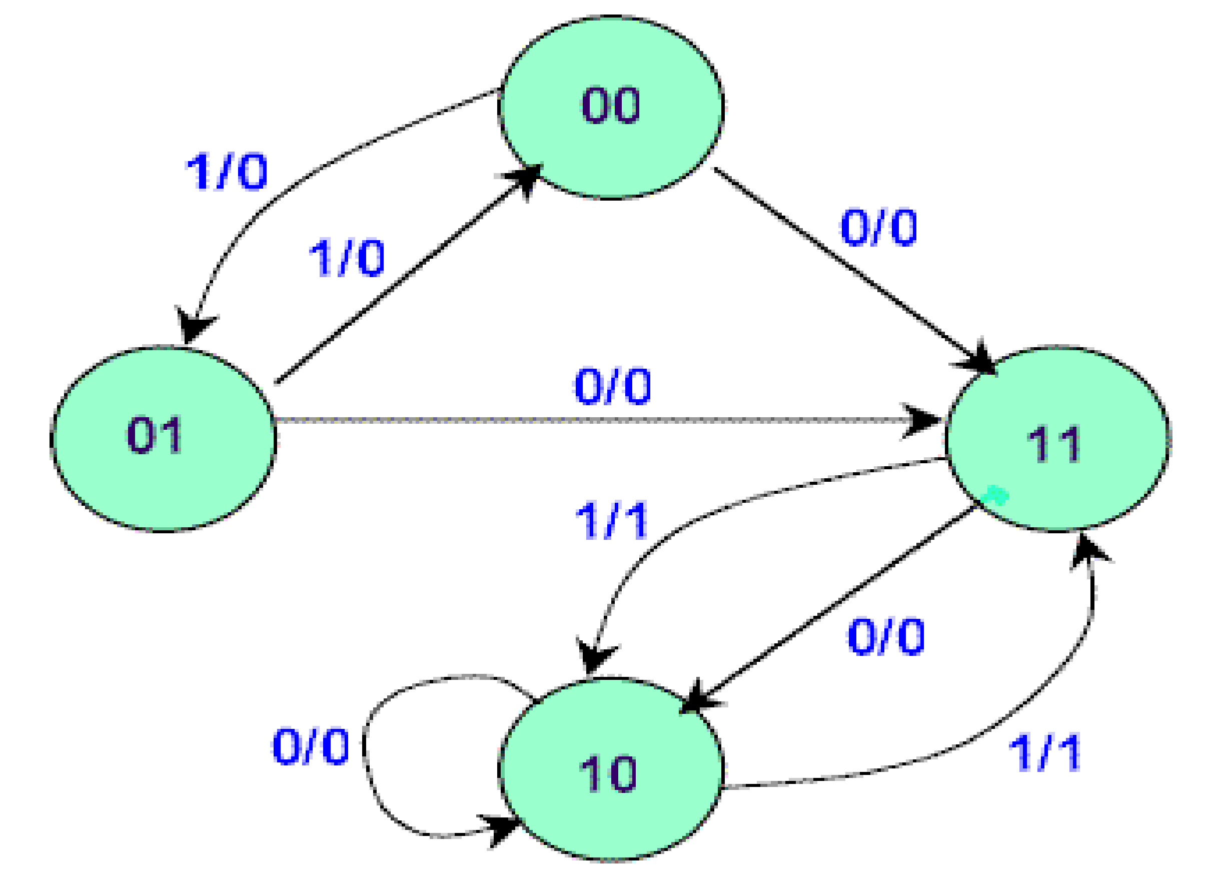
Present State	Next State		Output	
	X=0	X=1	X=0	X=1
S0	S1	S2	0	0
S1	S3	S4	0	0
S2	S5	S6	0	0
S3	SB	SB	0	0
S4	SB	SA	0	0
S5	SB	SA	0	0
S6	SB	SB	0	0
SB	S0	S0	0	0
SA	S0	S0	1	0

Quiz

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
a	c	f	0	0
b	d	e	0	0
c	h	g	0	0
d	b	g	0	0
e	e	b	0	1
f	f	a	0	1
g	c	g	0	1
h	c	f	0	0

Next state and Output sequence for a given input stream

- If we are given a specific sequence of inputs, the state diagram and/or state table, we can predict the sequence of states response to this input sequence and the output sequence too.
- Sequence of X = { 0, 0, 1, 1, 0, 1, 0}. Start state = (01).
- When X = 0 at state (01), then the next state is (11), and the output is 0.
- The next value of X = 0 and now we are at state (11), then the next state is (10), and the output is 0.
- The next value of X = 1 and now we are at state (10), then the next state is (11), and the output is 1.


00
01
11
10
1/0
1/0
0/0
0/0
1/1
0/0
0/0
1/1

If we have a sequence of X = { 0, 1, 1, 0, 0, 1, 1}.
Start state = (b).

Present State	Next State		Output	
	X=0	X=1	X=0	X=1
a	c	f	0	0
b	d	e	0	0
c	a	g	0	0
d	b	g	0	0
e	e	b	0	1
f	f	a	0	1
g	c	g	0	1